Sierra Components, Inc.

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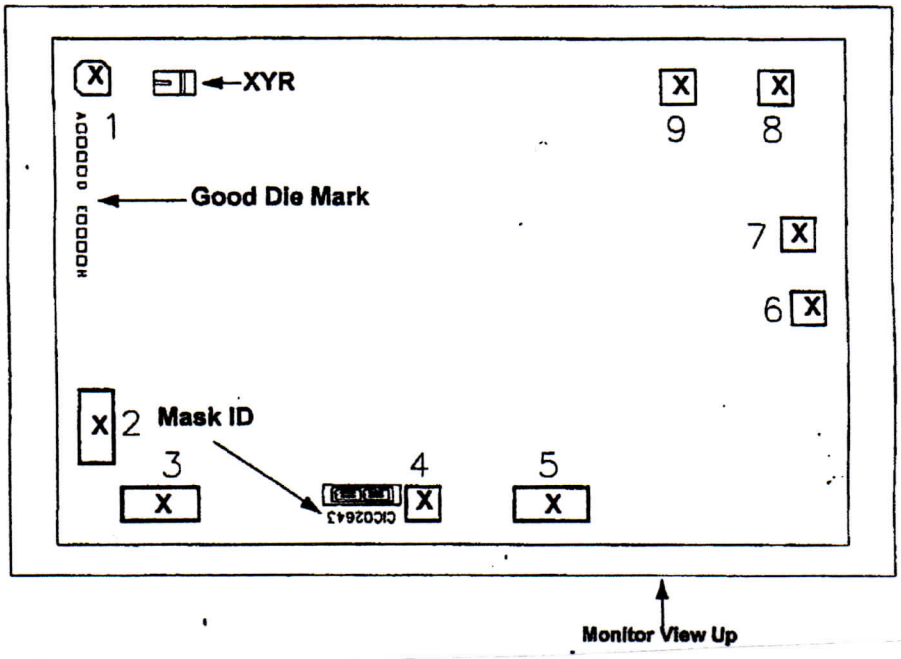
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



PAD LAYOUT TABLE

PAD #	PAD FUNCTION	PAD #	PAD FUNCTION
1	VDD	6	DGND
2	VREF	7	LD NOT
3	RFB	8	SRI
4	IOUT	9	CLK
5	AGND		

Top Material: Aluminum
Backside Material: Silicon
Bond Pad Size: .004" X .004" min.
Backside Potential:
Mask Ref:

APPROVED BY: DK	**DIE SIZE .070 x .110"**	**DATE: 6/7/16**
MFG: Texas Inst.	**TICKNESS .015"**	**P/N: DAC8043**